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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,530	GAREIS ET AL.	
	Examin r	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/04 amendments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/29/04,11/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are presented for examination.

Claim Objections

2. Claim 28 is objected to because of the following informalities: "output/output" should have been "input/output" at page 7, line 1. Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-3 and 9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 5,093,804 (hereinafter 804) in view of Wong et al (US Patent No 5,550,649).

The following language was added to claim 1 of the instant application:

> "wherein the I/O circuit comprises a switch processor, a plurality of signal conditioning circuits, and a switch section."

Patent 804 doesn't disclose about use of a processor to implement switch logic. However, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention in the patent 804 to have a more flexible, non-proprietary and easy to programmable/usable integrated circuit.

5. Claims 20-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6-13 of U.S. Patent No. 5,093,804 (hereinafter 804) in view of Wong et al (US Patent no 5,550,649) and Bowers et al (US Patent No 6,529,135). Independent claims 20, 23 and 28 of instant application are slightly different with disclosed independent claims 1, 6 and 9 of the patent 804 by addition of use of a firmware with the switch processor. As explained above, Wong et al clearly disclose that it is well known

in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Even though Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there would have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cieri et al (US Patent no 5,093,804[1]) in view of Wong et al (US Patent No 5,550,649).

8. As per claim 1, Cieri et al teach

generating in the controlling element a control signal in the form of sequential pulse frames, each frame having at least one control pulse defining said control information [col. 20, lines 10-13];

transmitting said control signal to said controlled element and generating in the controlled element a clock pulse for each control pulse such that said clock pulse follows said control pulse by a pre-selected time interval on each frame, there being one clock pulse for each control pulse such that there is a fixed time relationship between each control pulse and each clock pulse [col. 20, lines 14-21];

[1] Cieri et al is a prior art reference cited by applicants in IDS dated 10/16/01.

generating in the controlled element a diagnostic signal independent of the control signal but which is indicative of operating parameters of the controlled element [col. 20, lines 22-25]; and

using said clock pulse on each frame to cause a sampling of said control information and to cause a transmission of a value of said diagnostic signal to said controlling element [col. 20, lines 26-29].

Cieri et al do not disclose about a switch processor. However, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

9. As per claim 2, Cieri et al teach that each frame of the control signal further includes a no-pulse time interval during which no pulses appear defining the end of a frame [col. 20, lines 30-33].

10. As per claim 3, Cieri et al teach that each frame of said control signal includes a series of pulses defining said control information [col. 20, lines 34-36].

11. As per claims 4-8, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about the series of pulses comprising two to six pulses. But, Cieri et al clearly disclose that the series of pulses can contain either two or four pulses [col. 8, lines 25-27]. However, a routineer in the art would know to increase or decrease the number of pulses as needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the series of pulses to contain two to six pulses instead of two to four. Moreover, having extra pulses will allow one to provide some extra information as needed.

12. As per claim 9, Cieri et al teach that series of pulses is pulse width modulated [col. 20, lines 37-38].

13. Claims 10-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cieri et al (US Patent no 5,093,804) in view of Wong et al (US Patent no 5,550,649) and Bowers et al (US Patent No 6,529,135).

14. As per claim 10, Cieri et al teach that diagnostic signal comprises a multi-bit digital signal and the number of bits transmitted to said controlling element on each frame equals the number of pulses in said series of pulses in the same frame [col. 20, lines 39-43].

Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the

processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

15. As per claim 11, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

16. As per claim 12, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about the series of pulses comprising two to six pulses. But, Cieri et al clearly disclose that the series of pulses can contain either two or four [col. 8, lines 25-27]. However, a routineer in the art would know to increase or decrease the number of pulses as needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the series of pulses to contain two to six pulses instead of two to four. Moreover, having extra pulses will allow one to provide some extra information as needed.

17. As per claim 13, Cieri et al disclose that the switch processor comprises a zero crossing turn-on and turn-off feature [Fig. 8; col. 13, lines 61-64].

18. As per claim 14, Cieri et al disclose the invention substantially. Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly

disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

19. As per claim 15, Cieri et al teach that the switch processor receives a signal representative of the switch section current [Fig. 4; col. 11, lines 18-33].

20. As per claim 16, Cieri et al teach that the switch processor causes the switch to be turned off immediately upon detection of a first threshold current level [Fig. 4; ON/OFF; col. 11, lines 18-33].

21. As per claim 17, Cieri et al teach that the switch processor causes the switch to be turned off after a predetermined period of time [col. 14, line 51 – col. 15, line 19; Fig. 4].

22. As per claim 18, Cieri et al teach that the switch processor reports an overcurrent diagnostic signal, but does not turn off the switch, upon detection of a switch current level of a third threshold level, the third threshold level being lower than the second threshold level [Fig. 10].

23. As per claim 19, Cieri et al teach that the switch processor generates diagnostic codes for one or more of: over temperature conditions, short circuit conditions, over current conditions, low voltage conditions, and high voltage conditions based on input signals from the conditioning circuits [Fig. 10].

24. As per claim 20, Cieri et teach

at least one I/O point connected to the operations control unit and having an output control device subject to activation and deactivation as an operative condition in accordance with said control status and further including: (1) timing means responsive to each control pulse to generate a clock pulse which follows said control pulse by a pre-selected time interval on each frame, there being one clock pulse for each control pulse such that there if a fixed time relationship between such pulses; (2) means connected to the I/O point for providing a diagnostic signal having a value indicative of the operative condition of the I/O point; (3) means connected to receive each clock pulse and responsive to each clock pulse on each frame to cause a sampling of each control pulse to determine the desired control status; and (4) means connected to receive each clock pulse and the diagnostic signal and responsive to said clock pulse on each frame to cause a transmission of a value of said diagnostic signal to the operations control unit [col. 20, line 50 – col. 21, line 2].

Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

25. As per claim 21, Cieri et al teach that operations control unit provides said control signal such that each frame includes a series of pulses followed by a no-pulse time interval during which no pulses occur, said no-pulse time interval defining the end of a frame [col. 21, lines 3-7].

26. As per claim 22, Cieri et al teach that at least the first two pulses of each frame are pulse width modulated redundantly to determine the control status [col. 21, lines 8-10].

27. As per claim 23, Cieri et al teach

output control means responsive to be activated and deactivated by a command signal [col. 21, lines 16-17];

an operations controller generating at least one control signal in the form of sequential pulse frames, each frame of which contains at least one pulse defining a control status for the output control means and a time interval without pulses defining the end of the frame whenever said interval reaches a first pre-selected time duration [col. 21, lines 18-24];

a communications and control section receiving said control signal and including means responsive to said at least one pulse to provide said command signal for activating and deactivating said output control means in accordance with said control status for each frame and means responsive to said time interval for synchronizing operation of said communications and control section with each frame; sensing means providing status signals indicative of the operative condition of said output control means [col. 21, lines 25-35]; and

Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

28. As per claim 24, Cieri et al teach that each frame of said control signal contains a series of pulses defining said control status [col. 21, lines 43-45].

29. As per claim 25, Cieri et al teach that at least the first two pulses of each frame are pulse width modulated redundantly to determine the command signal for activating and deactivating the output control means [col. 21, line 46 – col. 22, line 2].

30. As per claim 26, Cieri et al teach that communications and control section further includes second selector means responsive to said time interval to cause said output control means to assume a pre-selected state whenever the time duration of said interval reaches a second pre-selected value [col. 22, lines 3-8].

31. As per claim 27, Cieri et al teach that a plurality of output control means and a corresponding plurality of communications and control sections, and wherein said operations controller generates a plurality of control signals providing one control signal for each communications and control section [col. 22, lines 9-14].

32. As per claim 28, Cieri et al teach

generating in the controlling element a control signal in the form of sequential pulse frames, each frame having at least one control pulse defining said control information [col. 20, lines 10-13];

transmitting said control signal to said controlled element and generating in the controlled element a clock pulse for each control pulse such that said clock pulse follows said control pulse by a pre-selected time interval on each frame, there being one clock pulse for each control pulse such that there is a fixed time relationship between each control pulse and each clock pulse [col. 20, lines 14-21];

generating in the controlled element a diagnostic signal independent of the control signal but which is indicative of operating parameters of the controlled element [col. 20, lines 22-25]; and

using said clock pulse on each frame to cause a sampling of said control information and to cause a transmission of a value of said diagnostic signal to said controlling element [col. 20, lines 26-29].

Cieri et al do not expressly disclose about a switch processor. But, Wong et al clearly disclose that it is well known in the art how to implement a switch processor [Fig. 2, 3; col. 5, line 67 -- col. 6, line 7; a number of switches that are controlled by a processor including input/output circuit]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize the advantages of the available knowledge of a switch processor and modify the disclosed invention by Cieri et al to have a more flexible, non-proprietary and easy to programmable or usable integrated circuit.

Cieri et al and Wong et al do not expressly disclose about a firmware used with the switch processor, a routineer in the art would know that it is quite obvious that there should have been a firmware with the processor to control the switches. However, Bowers et al clearly disclose that the knowledge to use a firmware with a processor to control a number of switches is well known in the art [Fig. 3; col. 6, lines 50-52, 55-56, 65-66; the switches are controlled by the processor according to the firmware instructions]. Therefore, it would have been obvious to one of ordinary skill in the art to utilize a firmware with a switch processor to control a number of switches.

Response to Arguments

33. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
December 29, 2004

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